Chips **2D** Processing and Visualization. **Modules**.

• *Types of modules.*

The 2D conveyor for Processing and Visualization consists presently out of 4 modules, each of them can be used both as stand-alone product and in any combination with each other – from two to all modules combine together:

1. Chip / Module for input stream of frames from HR digital cameras - **IP.4k**.
2. Chips / Modules for preliminary stream graphic data processing (frames) - **PP.4k**.
3. Chips / Modules for completion of stream processing (post-processing) of graphic data (frames) - **FP.4k**.
4. Chip / Module for display mapping of the HR graphic data (HR frames) - **VP.4k**.

For all technical applications, that include operating of HR digital cameras (and first of all – those without losses) the issue of raw data preparation is of primary importance.

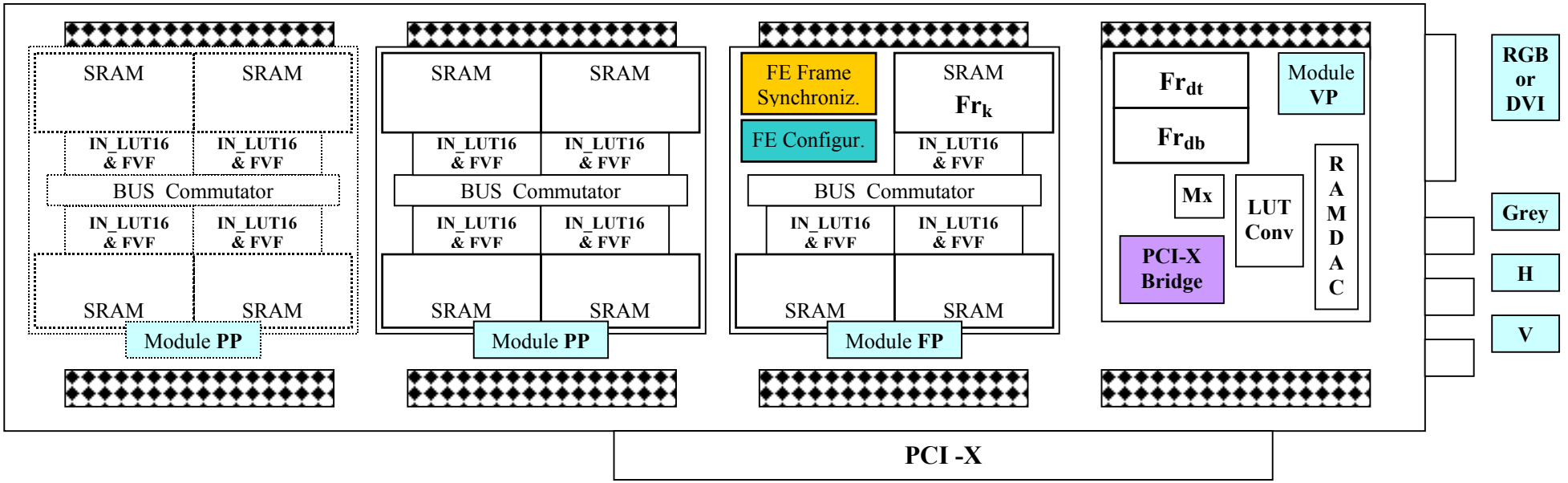
On another hand there are some technical applications, which operate with loss of raw data (using compression algorithms with loss of a source information and where complete data recovery is not possible!). In such cases serious data processing is not applicable, since it reveals all noises inherited by image from data compression.

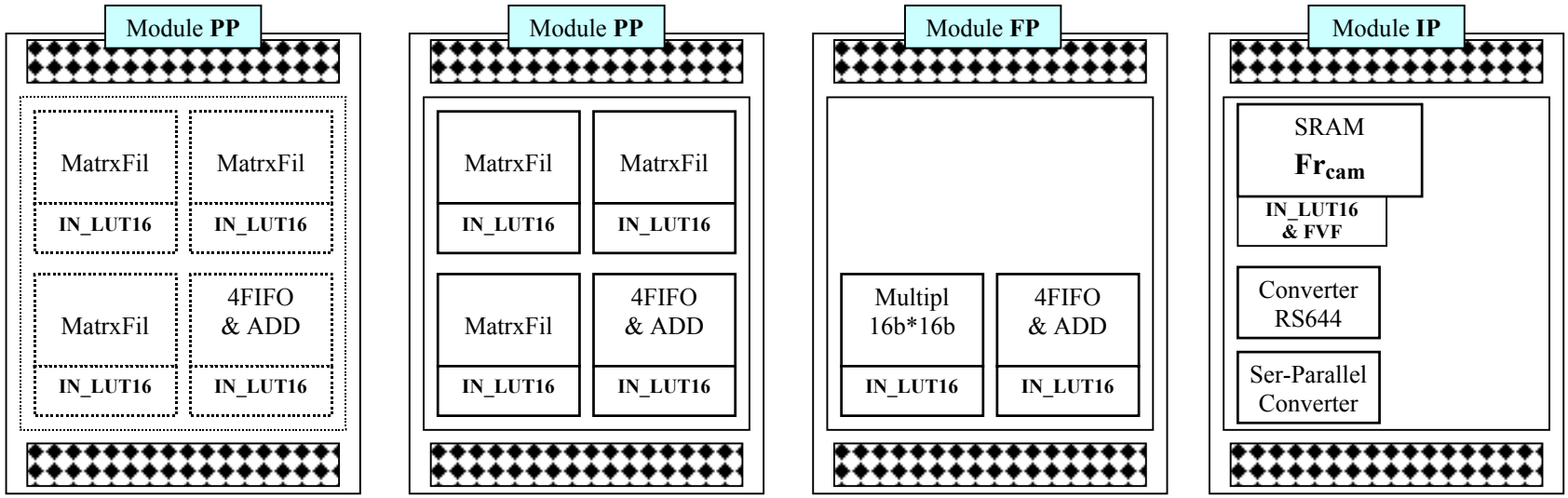
- Scalability at quantitative level (1,3,4 …..) for channels performing synchronous processing. The parallelism is provided at hardware level by building up identical conveyor for each channel and unified synchronization at hardware levels for all channels.

- All three modules for data manipulation feature the aforementioned scalability implemented at more than one computer. It is possible to organize a synchronous parallel operation of several channels at hardware level for several standalone computers. Thus it allows a vast number of modules combinations either up to all three together or, in some cases, similar modules can be implemented more than one in number per each channel. The synchronization is carried out by three main signals - frames frequency, lines frequency and clock (pixel) frequency. The unified data handling is carried out at each computer independently under setup parameters of conveyor and data arrays required for this or that operation of the channel to be carried out by each separate computer.

- Modules, from which the whole system is being assembled and tailored to customer demand, are being adapted for each new task by reconfiguration through the bus commutator of conveyor links, i.e. by substitution of the necessary Functional Element (FE) in the specified segment of conveyor whereas the management system loads necessary parameters and arrays depending on an input data type and on mathematical tasks to be performed for particular case of data processing.

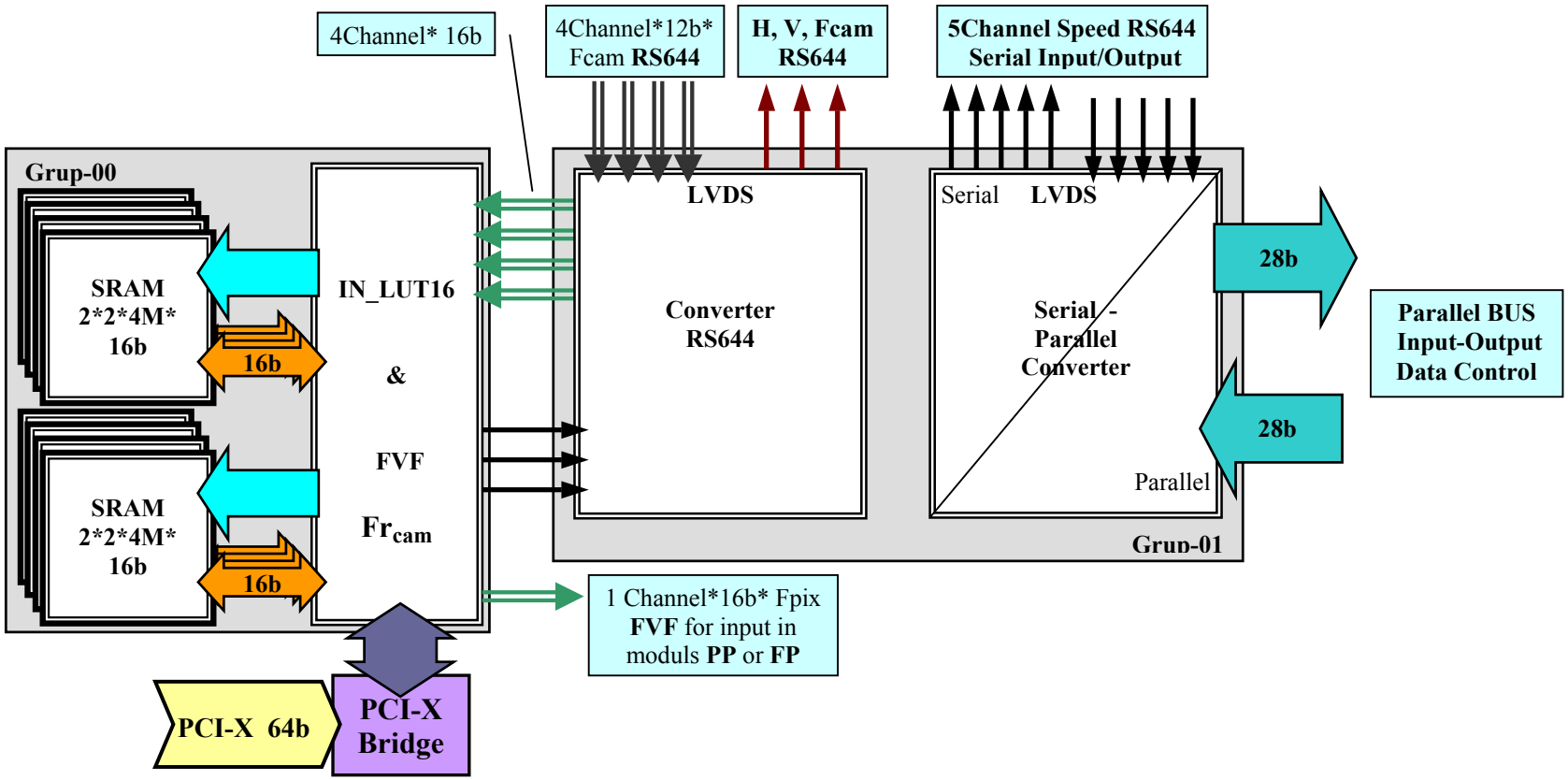
- ***The architecture of assembly of modules of the conveyor of 2D-Processing and Visualization & modules.***





All modules, except configuration functional elements and frame synchronization for display visualization fit into “mezzanine” architecture. Such construction implies subdivision of elements placement at mezzanine (processing elements) and on mainboard (communication/link elements with frame memory arrays and handling elements). Mezzanine also features module of synchronous input from digital camera.

• *The module of a parallel digital input of frames of the conveyor of 2D-Processing (Module Input Processing)*



Entry frames FE **FVF** $\mathbf{Fr_{cam}}$ represent doubled memory buffers, each capable to hold the full frame. The buffers are organized in four blocks to ensure synchronous data input obtained from converter module that performs conversion of **RS644 4x12b** channels to **4x16b** data channels. If the output data goes to **PP** or **FP** modules then the buffers are built as follows: one **16b** frame buffer block with one **16b** channel for data output each and operating at frequency **Fpix**.

Difficulties may occur as different digital cameras have the different technology of multichannel output from sensor matrix, with initially separated and mutually independent output signals, such peculiarity demands more flexible addressing procedure compared to standard element FE **FVF** (description of the element follows).

The total channel delay with parallel data input from the digital camera makes 1 frame.

The following chips TI SN65LVDS94 and SN65LVDS93 are prototype for FE **Ser/ParConv** and convert 28b parallel code at frequency 20-65 MHz into 4 serial differential channels (plus one differential clock channel) at frequencies up to 1.8 GHz.

Prototype for FE **ConvRS644** are the following chips:

- TI SN65LVDS386, converting 16 differential **RS644** channels into **16b** logical signals;
- TI SN65LVDS391, converting **4b** logical signals into 4 differential **RS644** channels.

• The Chips / Modules of preliminary stream processing of graphics frames.

Assignment of the module:

- The primary (main) task for digital primary HR sensors of any type is alignment of nonuniformity of sensitivity a pixel on all image field in cases when there be no further stream pixel normalization operations.
- The second task for digital primary HR sensors of any type is alteration of signal to noise ratio (S/N) either at the level of frame (pixel) operations by changing the resolution, or by manipulations between frames (time/frequency). The mode of operation with data accumulation allows receiving better results, then provided electronically at physical data retrieval.
- The third task - manipulations at input level between frames in real-time for special classes of stream frame processing.

It is important to state that the task to process dataflow **1к*1к*16b** at frequency from 25-30 up 50-60 frame/sec in real time, which is the first and foremost challenge today, is not resolved by any corporation. The solutions suggested imply careful selection of several sensors with close specifications and such solutions result finally in considerably higher prices of digital sensors for end-buyer.

The only exception makes computer thomograph (**CT** Scanning System), where re-calculation of pixel non-uniformity coming from sensors is carried out at apparatus workstation, otherwise it becomes impossible to obtain the image map due to of substantial non-uniformity of raw data coming from both internal set of x-ray detectors, as well as between the sensor sets. The task is solved by post-processing methods rather than by real-time electronics engineering.

In cases with preliminary normalization, there is possibility to implement greater number of sensors with less rigid tolerance parameters, and hence making it cheaper.
In case module is used in 2D conveyor processing it significantly improves S/N ratio of input data.

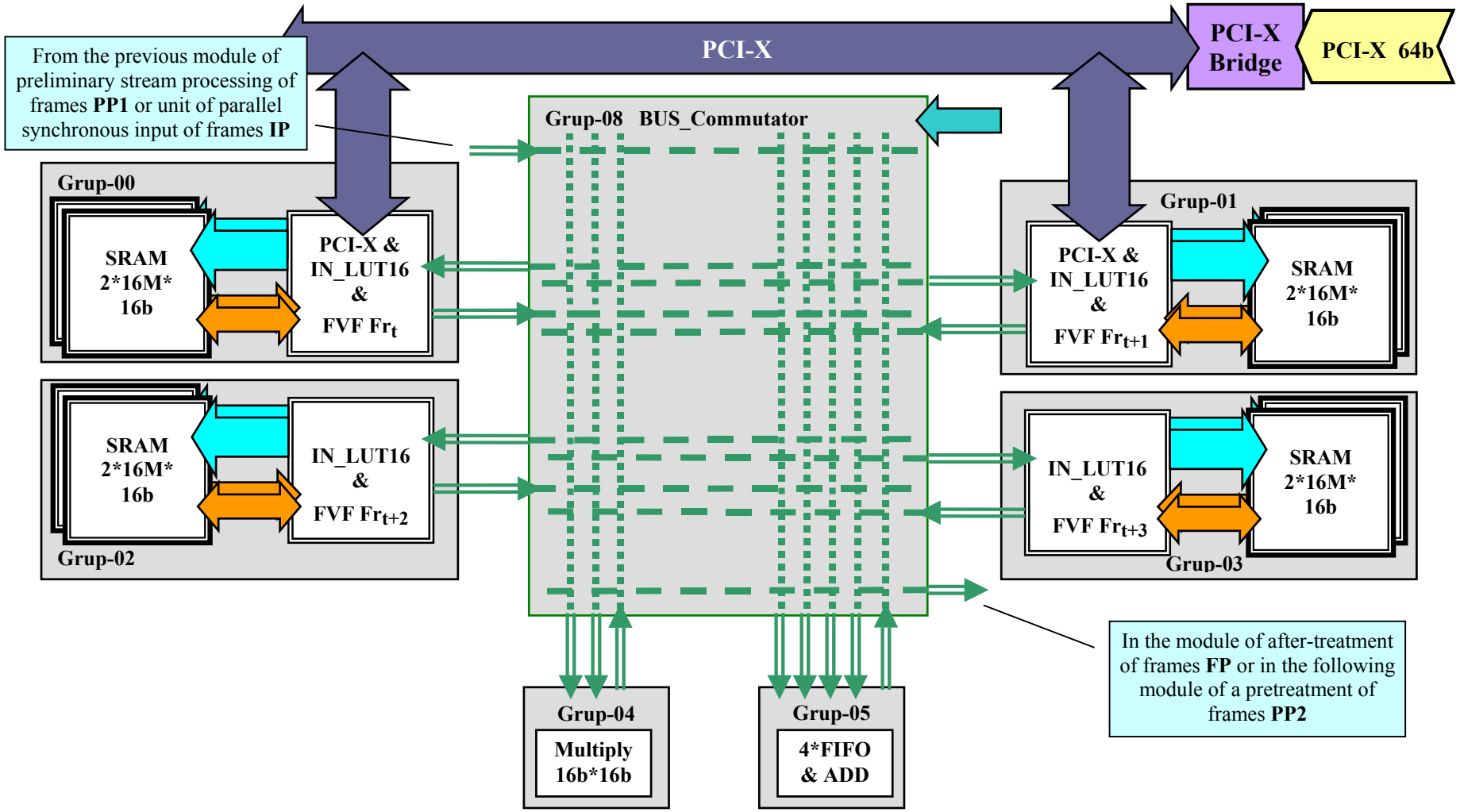
Examples of application

1. For the digital **2k*2k/30fps** cameras with output based on 4 **1k*1k** matrixes with and 4 parallel **12b*40MHz** channels. Module is used to normalize non-uniformity between matrixes in parallel stream.
2. Medical computer tomographers (CT) feature essential non-uniformity of raw data from x-ray detectors, both between sets of sensors and inside one set. The solution is in electronics engineering.
3. Correction of non-uniformity of luminosity at digitization of film frame, both for entire frame field or between frames of same film together with simultaneous gamma correction of RGB model.
4. Roentgenology features digital Flat panels up to 4k*4k and larger with the size 430*430мм, where the alignment of pixel non-uniformity caused by geometrical discrepancies needs to be solved, additionally the task to minimize time of calculation to facilitate rapid filming operation required by medical technologies, based on in-between frames manipulations.
5. In a Roentgenology where the regimen of dynamic integration of frames for pseudo-static objects is applied, thus the signal to noise ratio S/N is improved during dynamic frame visualization.
6. **DSA** (Digital Substraction Angiography) in a Roentgenology, with the subtraction of frames without contrast from stream of frames with contrast, thus enabling to single out the vascular system only.

Potential customers: (2k*2k is minimally required resolution for all applications enumerated above)

1. Manufacturers of X-Ray systems and diagnostic equipment;
2. Apparatuses and systems of digitization of films;
3. Microscopes with colour and black-and-white HR digital cameras;
4. Digital cameras in systems with high and super high resolution.

- ***The module of preliminary stream 2D-Processing of frames (Module Primary Processing).***



The input frame buffer FE **FVF Fr_t** and up to output frame buffer FE **FVF Fr_t** is double memory buffers, each of the full frame format.

They perform correction of non-uniformity of a pixel, where the correction coefficients **Fr_c** and **Fr_s** which are calculated for each pixel, or in the process of adding four sequential frames with independent coefficients for each frame. And the last module (FE **FVF Fr_t**) by the way, may become an initial part of final stream processing of frames. In both cases and for all four frames the pixels selected for mathematical operations should have identical coordinates **H_L** и **V_k**!! - i.e. frame buffers should have full data sets for all four frames simultaneously!

The maximum delay of data output at the module **PP** if performing correction of pixel non-uniformity makes 1 frame, and with frame adding it makes 2 frames.

Two units **PP** can work sequentially to perform conveyor processing, in such cases the delay will make 3 frames.

• The Chips / Modules of completing stream processing of graphics frames.

Assignment of the module:

- Continuation of stream data processing obtained from primary stream data processing procedure, to be performed at the module of completing stream processing in a real-time or in pseudo real-time modes.
- Stream processing of data obtained from digital sensors of the system, for stream processing in real-time or pseudo real-time modes.

1.1 Depending on manipulation types the completing stream processing itself can divided to:

a) Conveyor for processing of sequential frame stream;
б) Manipulation between frames with the subsequent conveyor processing, generally applied for two streams of frames.

1.2. Procedures at completing stream processing can be divided by their type to the following:
(Including any combinations for all types and sorts).

a) Processing of series of frames stream in real-time and for complete frame field;
б) Processing of several selected frame zones in frame series or processing of several different zones in different frames in a sequence simultaneously both in pseudo real-time and real time modes.

1.3. By technical implementation:

a. Hardware for real-time conveyor processing of B&W 16b images, in **2k*2k /(25-30) fps** matrix or **1k*1k** matrix at **(50-60)** or **(100-120) fps**.

b. In cases with three-channel processing - 48 bit RGB (16 bits/color) data with resolution **8Mpixel** at **25-30 fps**.

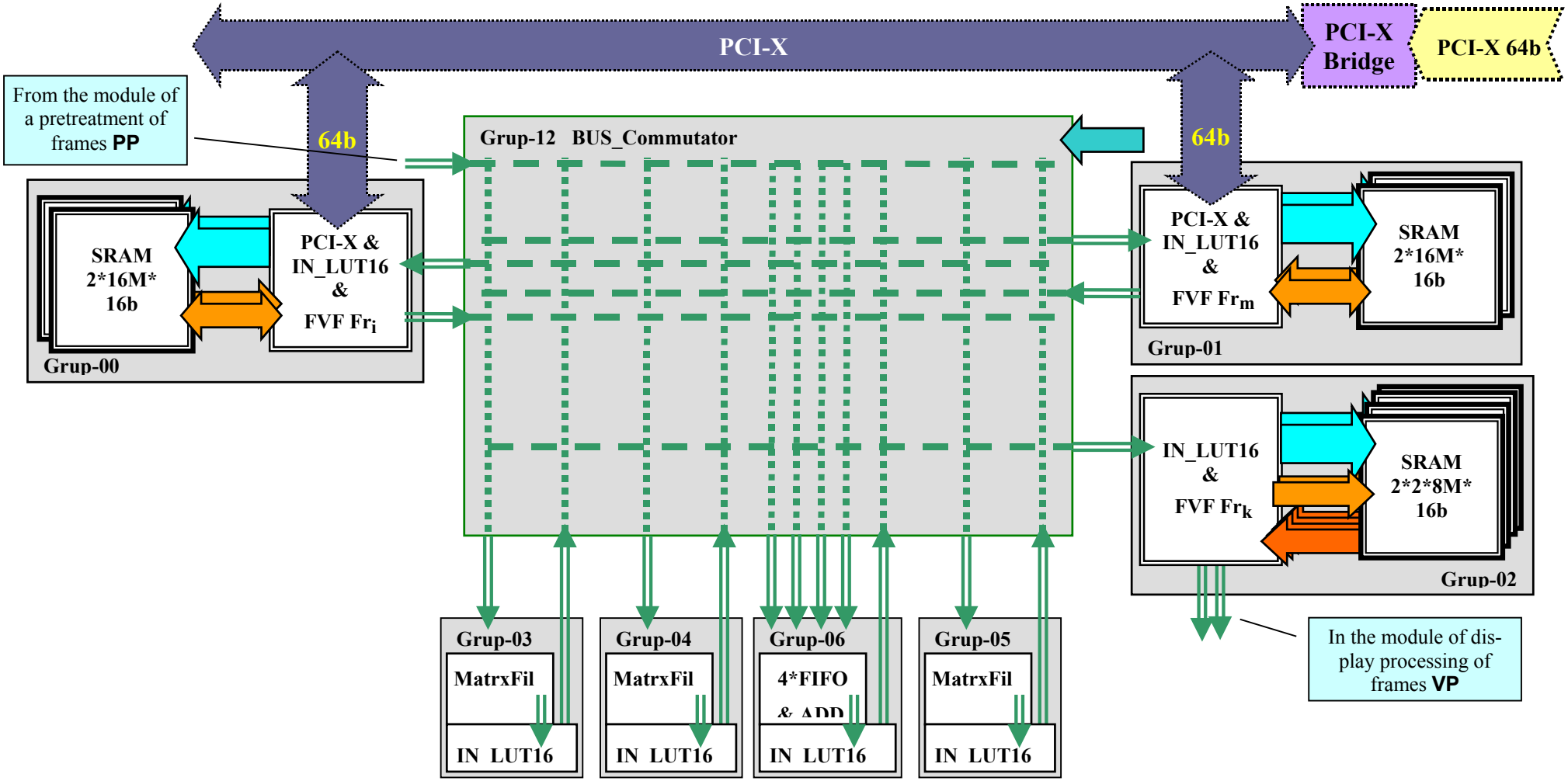
c. Same as in points a) and b) but only for the static images over **3k*3k**.

d. 2D hardware accelerator for processing of 16bit/color (48 (64) bit/pixel) images in graphics applications operating with the extra large images (with no limitation to image file size) in pseudo-real time mode.

Potential customers

1. Manufacturers of X-Ray systems and diagnostic equipment can be equipped with input module for preliminary processing for both static and dynamic operations:
2. Corporations that produce Digital apparatuses for X-Ray and digital Visualization systems based on **DICOM** standard.
3. Producers of apparatuses for both cine films digitization and systems of digital cine visualization (**D-Cinema**) with high-resolution.
4. Microscopes with color and black-and-white digital HR cameras:
5. The manufacturers of applications software for image processing that can be hardware accelerators based, due to complete evolution to 64-bit processors and calculations, thus enabling overall transition to 64 bit presentation of a pixel - that is 3*16b RGB plus 16b alpha channel. Such performance will substantially overload computation processor when operation with larger graphics files. In such cases it vital to implement 2D hardware acceleration for processing and visualization.

- ***The module of completing stream 2D-Processing of frames (Module Final Processing)***



The input frame buffers FE **FVF Fr_i** and FE **FVF Fr_m** in **FP** module are double memory buffers, each to the full frame format. They perform processes of subtraction with complete frames hence should be loaded with full frame data and should contain all frames necessary to perform subtraction procedure as frames required differ in timing and sequence.

The output frame buffer FE **FVF Fr_k** represents double memory buffer each to the full frame format and with the following capacities:

- For data input from final processing **FP** module a standard FE **FVF** with **16b** for each buffer and one **16b** data input channel is used,
- For data output to display processing **VP** module a non-standard FE **FVF** – the double frame buffer, each representing **2x16b** and two **16b** data output channel operating at double output speed to HR display window via **VP** module.

Any FE groups that are not used for conveyor processing can be suspended from operation, which contributes to higher flexibility.

• The Chip / Module of display stream mapping of graphics frames of superhigh resolution.

Assignment of the unit:

1. Output of data obtained from the conveyor after final stream processing to the HR screen monitor.
2. Operation as independent hardware product (graphic adapter) for output of graphics to HR screen monitors, best performance is achieved if combined with modules of final stream processing.

Independent implementation of two-component output to the screen in sync-mode operation:
- of user interface components (frames, sliders, indicators, selected parameters and so on) from HR display buffer (data loaded by computer processor) to HR monitor screen.
- dynamic output to the specified window, as set by controlling system processor, displaying a frame stream or a frame part synchronous to the HR display buffer, with format size limited by screen resolution.

Main display formats of HR CRT-screen monitors supported by the display mapping module - Clck = Fpix = Fdisp/ 2, where:
Fdisp - pixel output frequency to the screen,
Fpix - synchronous clock rate of FE module.

Quantity of pixels	H*V	VSync Hz	Color	Display output frequency Fdisp=2*Fpix (MHz)
8Mpix	3200 * 2560	48/50Hz	B&W	up to 500
5Mpix	2560 * 2048	50/(60)	B&W	up to 400 (450)
5Mpix	2048 * 2560	50/(60)	B&W	up to 400 (450)
4Mpix	1728 * 2304	50/60	B&W	up to 320
3Mpix	2048 * 1536	50/60/(75)	RGB	up to 280 (320)
2Mpix	1600 * 1200	50/60/75/(90)	RGB	up to 200 (240)
2Mpix	1400 * 1050	50/60/	B&W	up to 125

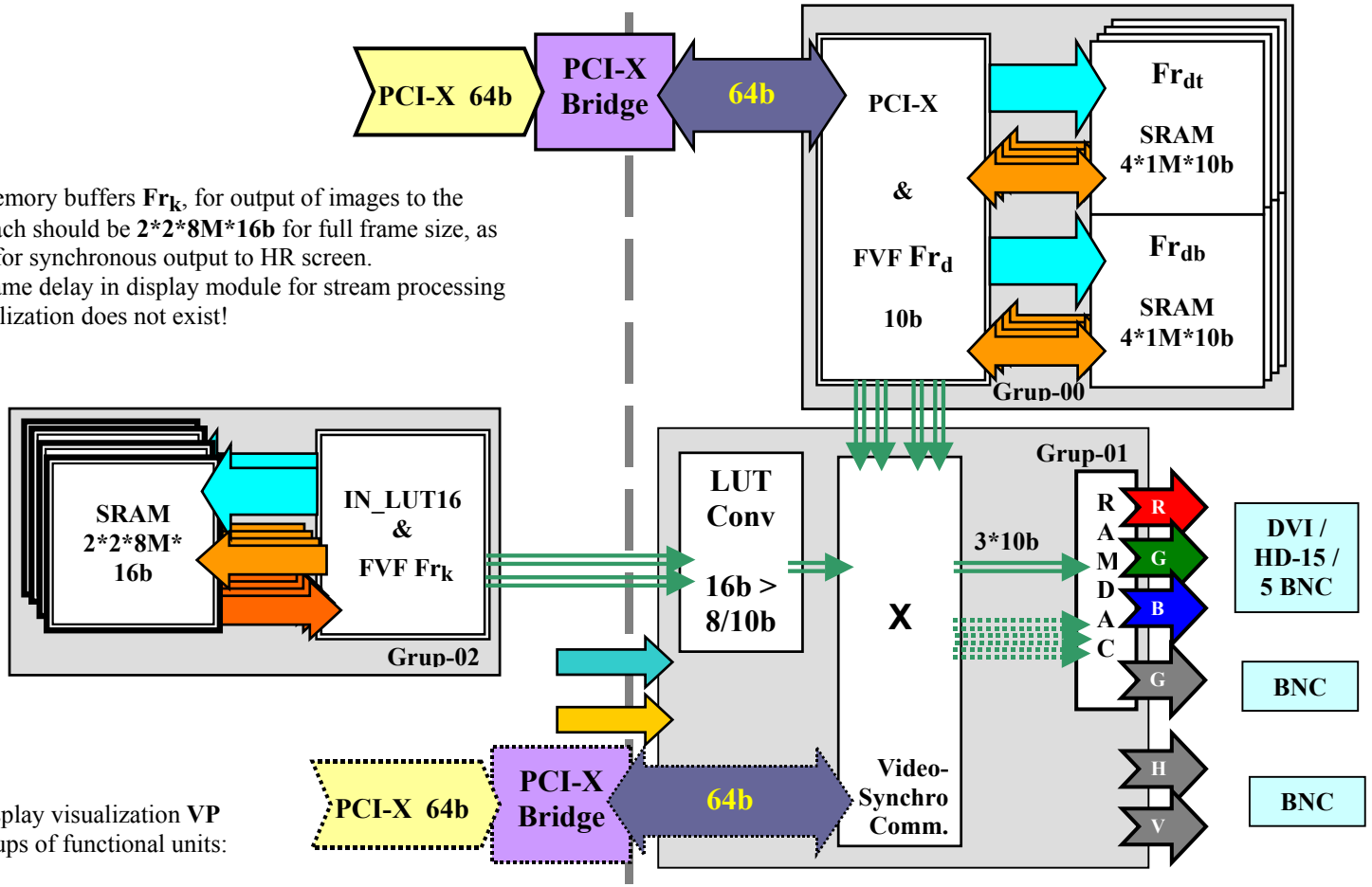
Potential customers:

All manufacturers of professional graphics adapters for HR and super high-resolution screen monitors.

• *The module of display stream 2D-Visualization of frames (Module Display Processing)*

The memory buffers **Fr_k**, for output of images to the screen, each should be **2*2*8M*16b** for full frame size, as required for synchronous output to HR screen.

The frame delay in display module for stream processing and visualization does not exist!



The module for display visualization **VP** consists of two groups of functional units:

- FE **FVF Fr_d** with **10b** display buffer designed to output to HR screen elements of graphics interface,
- The converter of data bit rate at FE **LUTConv** featuring video commutator FE **Video-Synchro** and **RAMDAC**, with **BNC** and **DVI/HD-15** at output.

The frame buffer **Fr_k** is loaded through two parallel **16b** channels at **Fpix/2**frequency; at the time of frame visualization **Fr_k** supports data output through two synchronous **16b** channels at **Fpix** frequency. The input data is loaded from FE **FVF Fr_k** to FE **LUTConv** by two synchronous **16b** channels at frequency of **Fpix.**
Output data is converted and transferred by one **10b** channel at **2Fpix=Fdisp** frequency to **10b RAMDAC** for output to HR display.

The display buffer is represented by FE **FVF Fr_d**, divided in to top and bottom blocks, grouped in 4 buffers with **16b** input-output channel each buffer. Display buffer data is loaded by **PCI-X** bus by computer processor only if interface is changed.

FE **Video-Synchro** supports cyclic synchronous output to **RAMDAC** of data stored in display buffer (do not confuse with frame buffer!).