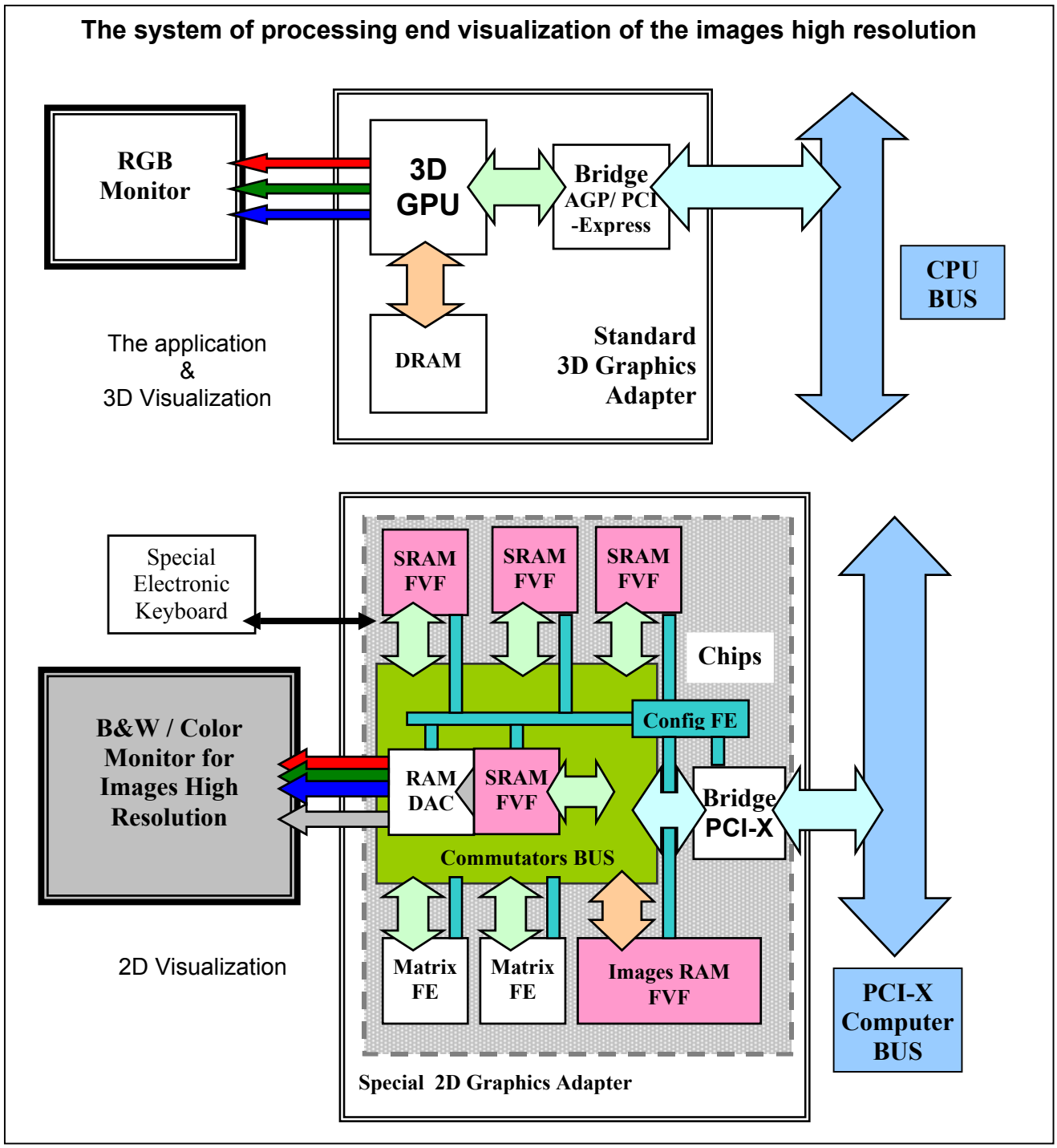
Chips **2D** Processing and Visualization of the images of super high resolution. **The Conveyor**.

• *The Conveyor 2D Processing and Visualization.*

Basically it is possible to subdivide HR image processing into the following types:

- **3D** Visualization (three-dimensional), including medical images, performed at professional graphics adapters with **3D-accelerators** running under appropriate operating system (for PC and compatible computers **3D AGP** or **PCI-Express** bus graphics adapter).
- **2D** Visualization (two dimensional) at high and super high resolutions, including medical images, performed by specialized graphics adapters "**2D Processing and Visualization**" with a set of chips designed to the philosophy "***Adaptive Systems 2D Processing and Visualization***".

The architecture of hardware product with separate systems of visualization **2D** and **3D** images.

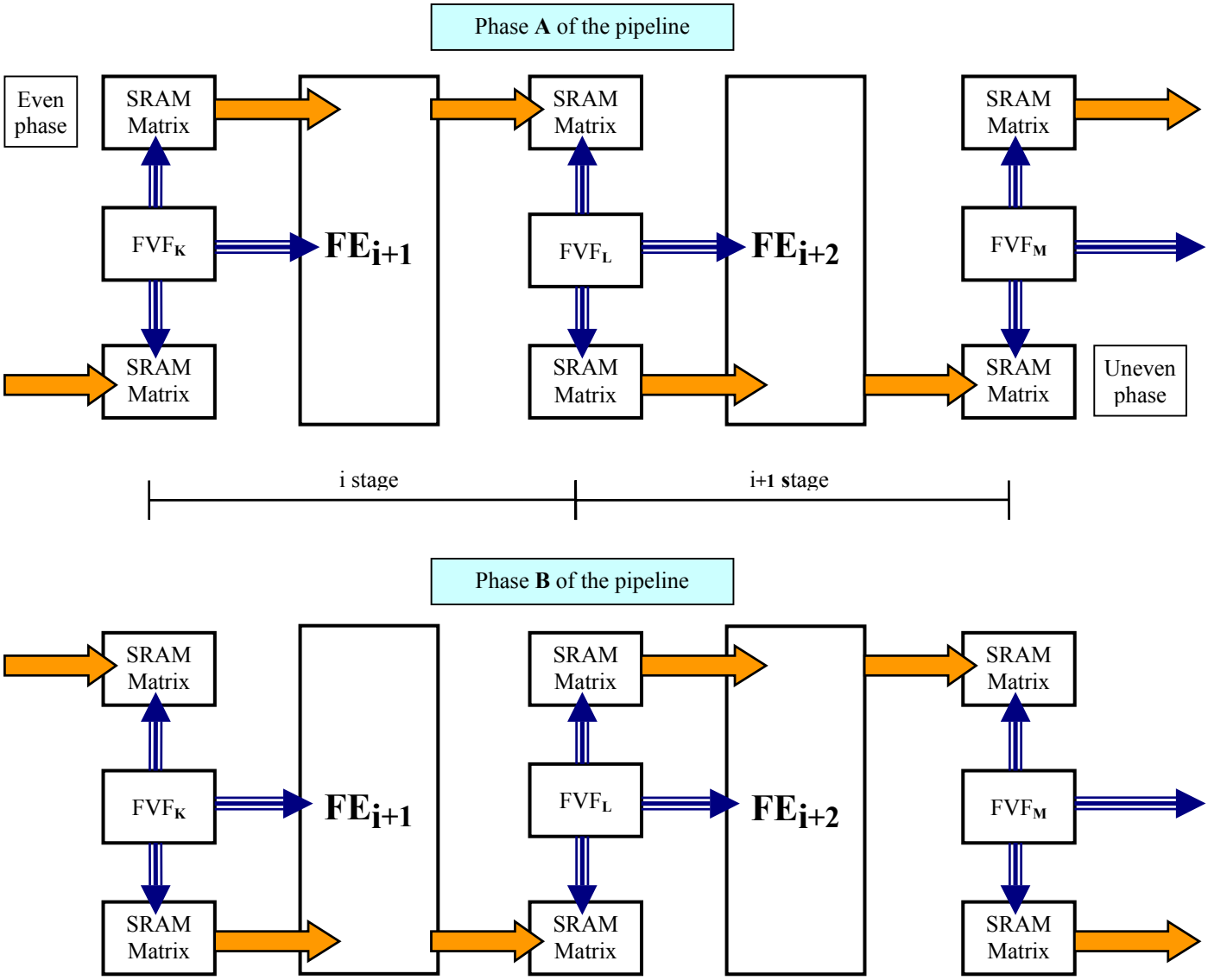


• *Operation of the Conveyor 2D Processing and Visualization.*

The common architecture of parallel-sequential calculations of an electronic part of the system "**2D Processing and Visualization**" can be described as odd and even phases of processing cycle in the parallel conveyor.
The interleaving phases form «*Peristalsises*» cycle of the conveyor.

The architecture allows to perform all conversion functions assigned and concentrated at Functional Elements - **FE** in parallel mode as the - **SRAM Matrix** – at each conveyor step is either receiving data obtained from the previous stage of conversion, or transmitting data to subsequent stage of conversion.

Thus input/output for buffer memory matrix is clearly divided both in time and in phase of conveyor cycle.



FE$_{i+1}$ and **FE$_{i+1}$** is set of Functional Elements (**FE**) that are used to build up the conveyor for **2D** processing and visualization in adaptive real-time systems.
FE are basic elements of conversion – the core for conversion processes - with functions that are either impossible or not desirable to split into smaller tasks.

The combination of FE sets and FE management system form ***The Electronic Technical Designer***.

In order to implement different tasks of **2D** processing and visualization FE are assembled in a conveyor, for configured data transfers in accordance to given stages and phases of processing. The visualization conveyor is launched and shut by user commands. The parameters of processing and visualization vary during system operation in periods between frames.

The organization of a continuous flow requires load and store intermediate results needed for the subsequent stage phase of frame processing:

- The result of processing is to be loaded to one buffer of a stage and should be uploaded to subsequent processing from another buffer at the same stage. So at each stage it is necessary to have two independent buffers with switching streams. The maximum size of each frame buffer makes **32MB**.
- At the final stage of conversion by FE the data for a selected zone of interest (or several zones) should be accumulated for the subsequent adjustment of spectrum and normalization in 16b range of the initial image.

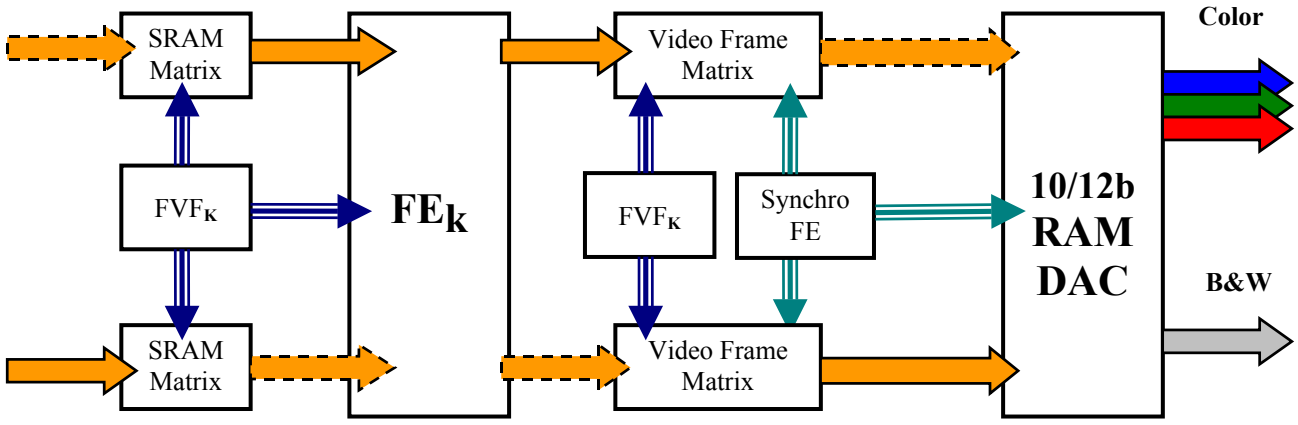
• *Output from the Conveyor for Visualization.*

For high speed output to HR screen monitors it is necessary to have double independent switched buffers of visualization of a processed frame.

To provide two and more outputs to HR screens monitors same set of double buffers is required with corresponding **RAMDAC: B&W 10(12)b / pixel** and / or **Color 10(12)b /** or **RGB 30(36)b / pixel**.

Independent setting of lines and frames frequencies for each screen monitor allows to precisely set up synchronization frequencies for HR professional screen monitors.

All conveyor operation rates are clocked to a rate of image output to HR screen monitor, the rates of processing FE should provide an in-sync system operation at frame synchronization level.



• *Data Input to the Conveyor of Processing and Visualization.*

The input to **2D** processing and visualization conveyor is carried out by **PCI-X** bridge to double buffer for the initial images - **Images RAM**, phased same as matrixes of buffer memory.

At larger sizes of the buffer for a series of initial images, the buffer can be organized directly in computer memory. With such organization of operation each buffer of the initial images performs as a matrix of buffer memory.